



# UTKAL INSTITUTE OF ENGINEERING & TECHNOLOGY

DISCIPLINE: ETC	SEMESTER: 4TH Sem	NAME OF THE TEACHING FACULTY: Er.Rehebari Tarannum		
<b>SUBJECT:</b> <b>Th.3 MICROPROCESSOR &amp; MICROCONTROLLE</b>		Semester From Date:16/01/2024 To Date:26/04/2024 No. Of Weeks: 15		
No of Days/Per week class allotted: 4 Class P/W(60)				
WEEK	CLASS DAY		REMARKS	
1 <sup>st</sup>	1 <sup>st</sup>	1.1 Introduction to Microprocessor and Microcomputer & distinguish between them	Date	Dean/Prin cipal
	2 <sup>nd</sup>	1.3 General Bus structure Block diagram.		
	3 <sup>rd</sup>	1.1 Data Communication		
	4 <sup>th</sup>	1.4 Basic Architecture of 8085 (8 bit) Microprocessor		
2 <sup>nd</sup>	1 <sup>st</sup>	1.5 Signal Description (Pin diagram) of 8085 Microprocessor		
	2 <sup>nd</sup>	1.6 Register Organizations, Distinguish between SPR & GPR, Timing & Control Module,		
	3 <sup>rd</sup>	1.7 Stack, Stack pointer & Stack top.		
	4 <sup>th</sup>	1.8 Interrupts:-8085 Interrupts, Masking of Interrupt(SIM,RIM)		
3 <sup>rd</sup>	1 <sup>st</sup>	1.3 General Bus structure Block diagram.		
	2 <sup>nd</sup>	1.1 Introduction to Microprocessor and Microcomputer & distinguish between them		
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4 <sup>th</sup>	1 <sup>st</sup>	1.5 Signal Description (Pin diagram) of 8085 Microprocessor		
	2 <sup>nd</sup>	1.6 Register Organizations, Distinguish between SPR & GPR, Timing & Control Module,		

	3 <sup>rd</sup>	Doubt Clear Class		
	4 <sup>th</sup>	2.1 Addressing data & Differentiate between one-byte, two-byte & three-byte instructions with examples.		
5 <sup>th</sup>	1 <sup>st</sup>	2.2 Addressing modes in instructions with suitable examples		
	2 <sup>nd</sup>	2.3 Instruction Set of 8085 (Data Transfer, Arithmetic, Logical, Branching, Stack & I/O, Machine Control)		
	3 <sup>rd</sup>	2.4 Simple Assembly Language Programming of 8085		
	4 <sup>th</sup>	2.4.1 Simple Addition & Subtraction		
6 <sup>th</sup>	1 <sup>st</sup>	2.4.2 Logic Operations (AND, OR, Complement 1's & 2's) & Masking of bits		
	2 <sup>nd</sup>	2.4.3 Counters & Time delay (Single Register, Register Pair, More than Two Register)		
	3 <sup>rd</sup>	2.4.4 Looping, Counting & Indexing (Call/JMP etc).		
	4 <sup>th</sup>	2.4.4 Looping, Counting & Indexing (Call/JMP etc)		
7 <sup>th</sup>	1 <sup>st</sup>	2.4.5 Stack & Subroutine programmes		
	2 <sup>nd</sup>	2.4.6 Code conversion, BCD Arithmetic & 16 Bit data Operation, Block Transfer.		
	3 <sup>rd</sup>	2.4.7 Compare between two numbers		
	4 <sup>th</sup>	2.4.8 Array Handling (Largest number & smallest number in the array) 2.5 Memory & I/O Addressing,		
8 <sup>th</sup>	1 <sup>st</sup>	2.4.5 Stack & Subroutine programmes		
	2 <sup>nd</sup>	2 Draw timing diagram for memory read, memory write, I/O read, I/O write machine cycle.		
	3 <sup>rd</sup>	3.3 Draw a neat sketch for the timing diagram for 8085 instruction (MOV, MVI, LDA instruction)		
	4 <sup>th</sup>	3.1 Define opcode, operand, T-State, Fetch cycle, Machine Cycle, Instruction cycle & discuss the concept of timing diagram.		
9 <sup>th</sup>	1 <sup>st</sup>	3.2 Draw timing diagram for memory read, memory write, I/O read, I/O write machine cycle.		
	2 <sup>nd</sup>	3.3 Draw a neat sketch for the timing diagram for 8085 instruction (MOV, MVI, LDA instruction).		

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10 <sup>th</sup>	1 <sup>st</sup>	3.3 Draw a neat sketch for the timing diagram for 8085 instruction (MOV, MVI, LDA instruction)		
	2 <sup>nd</sup>	SAMPLE PAPER QUESTION DISCUSSION		
	3 <sup>rd</sup>	4.1 Concept of interfacing		
	4 <sup>th</sup>	4.2 Define Mapping & Data transfer mechanisms - Memory mapping & I/O Mapping		
11 <sup>th</sup>	1 <sup>st</sup>	4.3 Concept of Memory Interfacing:- Interfacing EPROM & RAM Memories		
	2 <sup>nd</sup>	4.4 Concept of Address decoding for I/O devices		
	3 <sup>rd</sup>	4.5 Programmable Peripheral Interface: 8255		
	4 <sup>th</sup>	4.6 ADC & DAC with Interfacing		
12 <sup>th</sup>	1 <sup>st</sup>	4.7 Interfacing Seven Segment Displays		
	2 <sup>nd</sup>	4.8 Generate square waves on all lines of 8255		
	3 <sup>rd</sup>	4.9 Design Interface a traffic light control system using 8255. 4.10 Design interface for stepper motor control using 8255. 4.11 Basic concept of other Interfacing DMA controller, USART		
	4 <sup>th</sup>	5.1 Register Organisation of 8086		
13 <sup>th</sup>	1 <sup>st</sup>	5.2 Internal architecture of 8086		
	2 <sup>nd</sup>	5.3 Signal Description of 8086		
	3 <sup>rd</sup>	5.4 General Bus Operation & Physical Memory Organisation		
	4 <sup>th</sup>	5.5 Minimum Mode & Timings		
	1 <sup>st</sup>	5.6 Maximum Mode & Timings,		

14th	2 <sup>nd</sup>	5.7 Interrupts and Interrupt Service Routines, Interrupt Cycle, Non-Maskable Interrupt, Maskable Interrupt		
	3 <sup>rd</sup>	8 8086 Instruction Set & Programming: Addressing Modes, Instruction Set, Assembler Directives and Operators, 5.9 Simple Assembly language programming using 8086 instructions		
	4 <sup>th</sup>	6.1 Distinguish between Microprocessor & Microcontroller 6.2 8 bit & 16 bit microcontroller 6.3 CISC & RISC processor 6.4 Architecture of 8051 Microcontroller		
15th	1 <sup>st</sup>	6.5 Signal Description of 8051 Microcontrollers 6.6 Memory Organisation- RAM structure, SFR 6.7 Registers, timers, interrupts of 8051		
	2 <sup>nd</sup>	6.8 Addressing Modes of 8051 6.9 Simple 8051 Assembly Language Programming Arithmetic & Logic Instructions, JUMP, LOOP, CALL Instructions, I/O Port Programming		
	3 <sup>rd</sup>	6.10 Interrupts, Timer & Counters 6.11 Serial Communication		
	4 <sup>th</sup>	6.12 Microcontroller interrupts and Interfacing to 8255		

HOD

DEAN

PRINCIPAL

*Jyoti Prakash Swain*

*Chittaranjan Parida*

*(Signature)*